Ultra-low power consumption and high performance2.4GHz GFSKwireless transceiver chip

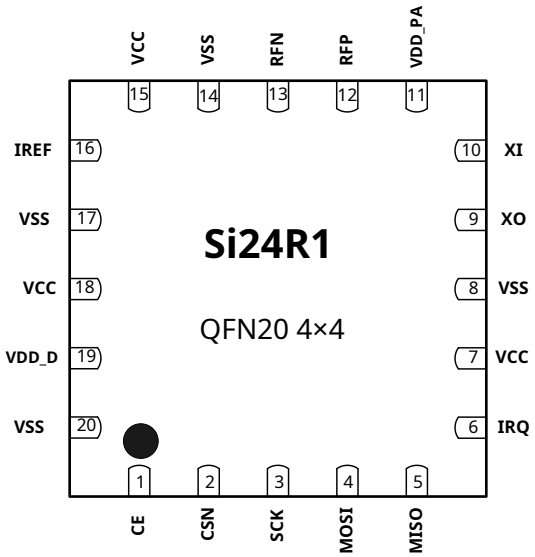
main features

- work at2.4GHz ISMfrequency band
- Modulation:GFSK/FSK
- Data rate:2Mbps/1Mbps/250Kbps
- Ultra-low shutdown power consumption:1uA
- Ultra-low standby power consumption:15uA
- Receive Sensitivity:-83dBm @2MHz
- Maximum transmit power:7dBm
- receive current (2Mbps):15mA
- emission current (2Mbps): 12mA(0dBm)
- High internal integrationPSRR LDO
- Wide Supply Voltage Range:1.9-3.6V
- wide numbersI/Ovoltage range:1.9-5.25V
- Fast boot time:≤ 130uS
- Highest10MHzFour linesSPIinterface
- Integrate IntelligenceARQBaseband Protocol Engine
- Send and receive data hardware interrupt output
- support1bit RSSIoutput
- Low cost crystal oscillator:16MHz±60ppm
- Very few peripheral components, reducing system application cost
- QFN20package orCOBencapsulation

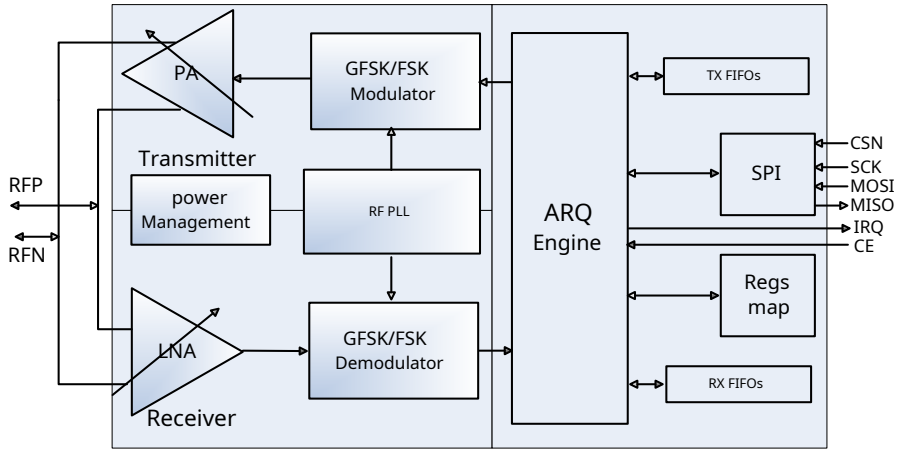
Application range

- wireless mouse, keyboard
- Wireless remote control, somatosensory equipment
- activeRFID,NFC
- Smart Grid, Smart Home
- wireless audio
- Wireless Data Transmission Module
- Low power ad hoc network wireless sensor network node

Package diagram



Structure diagram



term abbreviation

the term	describe	Chinese description
ARQ	Auto Repeat-reQuest	automatic retransmission request
ART	Auto ReTransmission	automatic resend
ARD	Auto Retransmission Delay	automatic retransmission delay
BER	Bit Error Rate	BER
CE	Chip Enable	chip enable
CRC	Cyclic Redundancy Check	Cyclic Redundancy Check
CSN	Chip Select	Chip Select
DPL	Dynamic Payload Length	Dynamic Carrier Length
GFSK	Gaussian Frequency Shift Keying	Gaussian frequency shift keying
IRQ	Interrupt Request	interrupt request
ISM	Industrial-Scientific-Medical	Industry - Science - Medicine
LSB	Least Significant Bit	least significant bit
Mbps	Megabit per second	megabits per second
MCU	Micro Controller Unit	microcontroller
MHz	Mega Hertz	megahertz
MISO	Master In Slave Out	Host input Slave output
MOSI	Master Out Slave In	Master output Slave input
MSB	Most Significant Bit	MSB
PA	Power Amplifier	power amplifier
PIDs	Packet Identity	packet identification bit
PLD	Payload	Carrier
RX	RX	Receiving end
TX	TX	The transmitting end
PWR_DWN	Power down	power down
PWR_UP	Power Up	Power-on
RF_CH	Radio Frequency Channel	RF channel
RSSI	Received Signal Strength Indicator	signal strength indicator
RX	Receiver	receiver
RX_DR	Receive Data Ready	Receive data ready
SCK	SPI Clock	SPIclock
SPI	Serial Peripheral Interface	Serial Peripheral Interface
TX	Transmitter	transmitter
TX_DS	Transmit Data Sent	sent data
XTAL	Crystal	crystal oscillator

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1Introduction

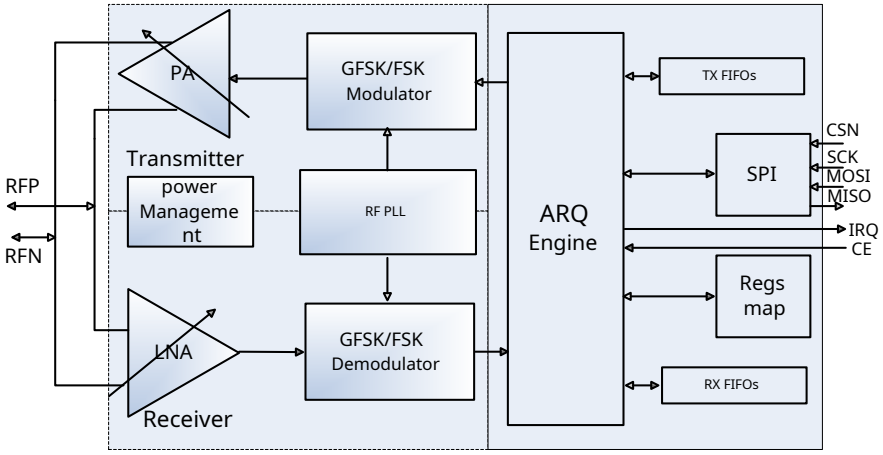
Si24R1is a working2.4GHz ISMfrequency band, designed for low-power wireless applications, integrated embedded ARQWireless transceiver chip for baseband protocol engine. The operating frequency range is2400MHz-2525MHz, in total126 indivual1MHzbandwidth channel. Internally integrates a high PSRR LDO power supply to ensure stability within a wide power supply range of 1.9-3.6V Work.

Si24R1useGFSK/FSKDigital modulation and demodulation technology. Data transmission rate can be adjusted, support 2Mbps, 1Mbps, 250KbpsThree data rates. High data rate can complete the same data in less time Transceiver, so can have lower power consumption. The output power of the chip can be adjusted, and the corresponding configuration can be adapted according to the actual application. Combined output power, saving system power consumption.

Si24R1Especially optimized for low-power applications, in shutdown mode, all register values are the same asFIFO value remains constant, the shutdown current is1uA; In standby mode, the clock remains active and the current is15uA, and can at the longest130uSStart sending and receiving data within the time.

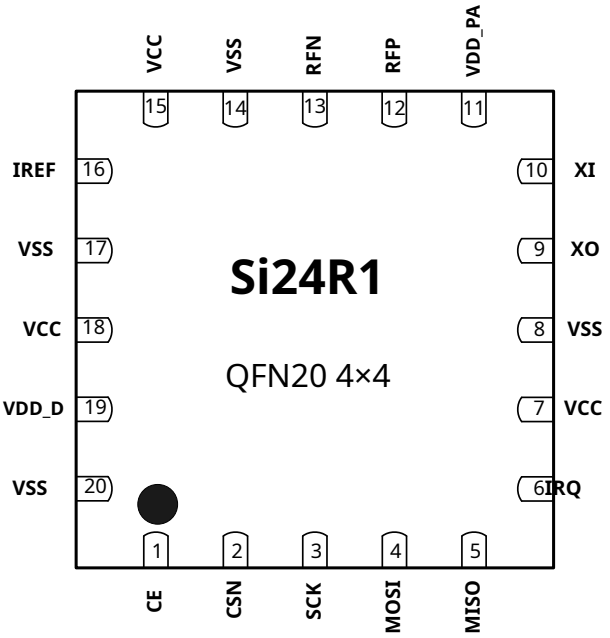
Si24R1Easy to operate, only needMCUpassSPIThe interface can be configured with a few registers on the chip Realize data sending and receiving communication. EmbeddedARQThe baseband engine is based on the principle of packet communication and supports multiple communication modes. manual or fully automaticARQProtocol operation. Internal integrated transceiverFIFO, to ensure that the chip withMCUContinuous data transmission, EnhancedARQThe baseband protocol engine can handle all high-speed operations, greatly reducingMCUsystem consumption.

Si24R1Has a very low system application cost, requiring only aMCUand a small number of peripheral passive components can Form a wireless data transceiver system. numberI/Ocompatible2.5V/3.3V/5Vand many other standardsI/Ovoltage, which can be compared with variousMCUThe ports are directly connected.



picture1-1Chip Structure Block Diagram

2Pin information



picture2-1 Si24R1Pin Infographic (QFN20 4x4package)

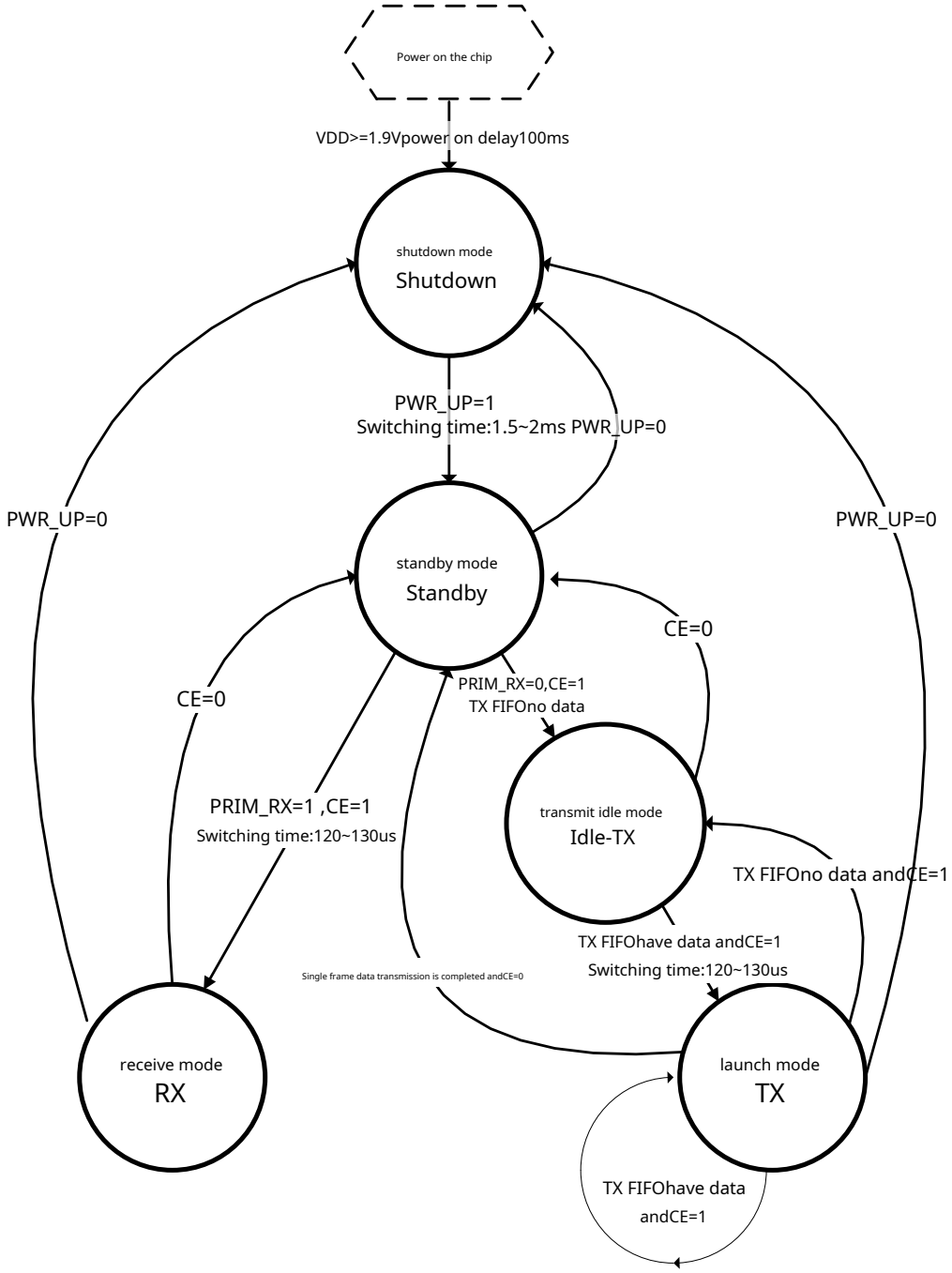
surface2.1Pin function description

port	port name	port type	Functional description
1	CE	DI	chip on signal, activateRXorTXmodel
2	CSN	DI	SPIchip select signal
3	SCK	DI	SPIclock signal
4	MOSI	DI	SPIinput signal
5	MISO	do	SPIoutput signal
6	IRQ	do	Maskable interrupt signal, active low
7,15, 18	VCC	power	power supply (+1.9 ~ +3.6V,DC)
8,14, 17,20	VSS	power	land(0V)
9	XO	AO	Crystal oscillator output pin
10	XI	AI	Crystal oscillator input pin
11	VDD_PA	power	to built inPApowered by the power output pin (+1.8V)
12	RFP	RF	Antenna interface1
13	RFN	RF	Antenna interface2
16	IREF	AI	Reference current
19	VDD_D	PO	Internal digital circuit power supply, decoupling capacitor must be connected
	Die exposed	power	land(0V), recommended withPCBconnected in a large area

3Operating mode

3.1state transition diagram

Si24R1There is a state machine inside the chip, which controls the transition of the chip between different working modes. Si24R1 can be configured asShutdown,Standby,Idle-TX,TXandRXFive working modes. The state transition diagram is shown in the figure 3-1shown.



picture3-1 Si24R1Working mode switching diagram

3.1.1 ShutdownOperating mode

existShutdownIn working mode,Si24R1All transceiver function modules are turned off, the chip stops working, and the current consumption is minimal, but all internal register values andFIFOThe value remains unchanged and can still be passedSPIRead and write registers. set upCONFIGregisterPWR_UPThe value of the bit is0, the chip immediately returns toShutdownOperating mode.

3.1.2 StandbyOperating mode

existStandbyIn the working mode, only the crystal oscillator circuit works, which ensures that the chip can start quickly while consuming less current. set upCONFIGunder the registerPWR_UPThe value of the bit is1, the chip enters after the clock is stableStandbymodel. The clock stabilization time of the chip is generally1.5~2ms, is related to the performance of the crystal oscillator. When the pin CE=1, the chip will consist ofStandbymode intoIdle-TXorRXmode whenCE=0, the chip will consist of Idle-TX,TXorRXmode returns toStandbymodel.

3.1.3 Idle-TXOperating mode

existIdle-TXIn the working mode, the crystal oscillator circuit and the clock circuit work. compared to Standbymode, the chip consumes more current. when the senderTX FIFOregister is empty, and the pinCE=1, the chip enters the Idle-TXmodel. In this mode, if a new packet is sentTX FIFO, the circuit inside the chip will start immediately, switching toTXmode to send packets.

existStandbyandIdle-TXoperating mode, all internal register values andFIFOThe value remains unchanged and can still be passedSPIRead and write registers.

3.1.4 TXOperating mode

When you need to send data, you need to switch toTXOperating mode. The chip goes intoTXThe working mode conditions are: TX FIFOThere is data inCONFIGregisterPWR_UPThe value of the bit is1,PRIM_RXThe value of the bit is0, while requiring the pinCElasts at least one10ushigh pulse.Idle-TXmode switch toTXThe mode time is120us~130usbetween, but not exceeding130us. After sending a single packet of data, ifCE=1,then by TX FIFOstate to determine the working mode of the chip, whenTX FIFOAs well as data, the chip continues to remain in TXworking mode, and send the next packet of data; whenTX FIFONo data, the chip returnsIdle-TXmode; ifCE=0, returns immediatelyStandbymodel. After the data transmission is completed, the chip generates a data transmission completion interrupt.

3.1.5 RXOperating mode

When you need to receive data, you need to switch toRXOperating mode. The chip goes intoRXThe conditions for the operating mode are: Set the registerCONFIGofPWR_UPThe value of the bit is1,PRIM_RXThe value of the bit is1, and the pinCE=1. chip byStandbymode switch toRXThe mode time is120~130us. When a packet is received with the address of the core

slice addresses are the same, andCRCWhen the check is correct, the data is automatically stored in theRX FIFO, and generate a data receive interrupt. The chip can store up to three valid data packets at the same time, whenFIFOis full, the received data packets are automatically discarded.

In receive mode, it is possible to pass theRSSIThe register detects the received signal power. When the received signal strength is greater than -60dBmhour,RSSIregisterRSSIThe value of the bit will be set to1. otherwise,RSSI=0. .RSSIThere are two ways to update the register: when a valid data packet is received,RSSIwill be updated automatically, in addition, changing the chip from RXmode switch toStandbymodeRSSIIt will also be updated automatically.RSSIThe value of will vary with temperature, and the range is ±5dBmwithin.

4packet processing protocol

Si24R1Based on packet communication, support stop equalityARQprotocol. inside the chipARQThe protocol baseband processing engine can be implemented automatically without the intervention of an external microcontrollerACKandNO_ACKPacket processing.ARQProtocol baseband processing unit support1arrive32The byte dynamic data length, the data length is in the data packet. Fixed data length can also be used, specified by the register; the baseband processing unit completes the automatic unpacking, packing and automatic reply of the data ACKAcknowledgment signal and automatic retransmission. Inside the processing unit are6a communication channel that can directly support1:6star network.

4.1 ARQpacket format

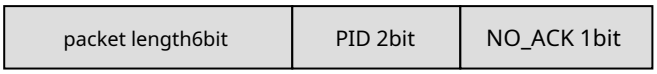
a completeARQThe packet includes preamble, address, packet control word, payload data, andCRC. as shown in the picture 4-1Shown as a complete package.

picture4-1a complete dataARQBag

The preamble field is mainly used for receiving data synchronization, the chip is automatically attached when transmitting, and the chip is automatically removed when receiving, which is invisible to the user.

The address field is the address of the recipient of the data, and it will be received only when the address is the same as the address in the address register of the chip. The address length can be configured by registerAWconfigured as3,or4,or5byte.

The length of the packet control field is9bit,The structure is shown in the figure4-2.



picture4-2Packet Control Field Format

The packet length subfield specifies the length of the packet, which can be0arrive32byte. For example:000000 = 0byte(package is empty)

100000 = 32 byte(The packet length is32byte)

PIDsThe subfield informs the receiving end whether the packet is a new packet or a retransmitted packet, which can prevent the receiving end from receiving the same packet multiple times. sender throughSPIWriteFIFO,PIDsThe value is automatically accumulated.

NO_ACKThe subfield is1, it means that the transmitter informs the receiver that there is no need to replyACK Acknowledgment signal. For the transmitter, makeNO_ACKBit is1Need to configure firstFEATUREin the registerEN_DYN_ACKBit is1, and useW_TX_PAYLOAD_NOACKcommand to writeFIFO. When such a packet is received, the receiver will not sendACK Acknowledgment signal to transmitter. (Even if the receiver is working onACKreceive mode)

The payload data field is the transmission data content, which can be as long as32byte.

CRCfield for the packageCRCvalue,CRCsupport8bitand16bittwo kinds,CRCthe length ofCONFIG

in the registerCRCObit configuration.

4.2 ARQcommunication mode

existTXIn this mode, the sender automatically sends the preamble, address, packet control word, payload data,CRCPack. The signal is modulated and transmitted through the antenna through the radio frequency module.

existRXIn this mode, the receiving end continuously detects the effective address in the received demodulation signal. Once the address is detected to be the same as the receiving address, it starts to receive data. If the received data is valid, the payload data is stored in the RX FIFO, and generate an interrupt notificationMCU.MCUpassSPIInterfaces are always accessibleRX FIFOregister for data reading.

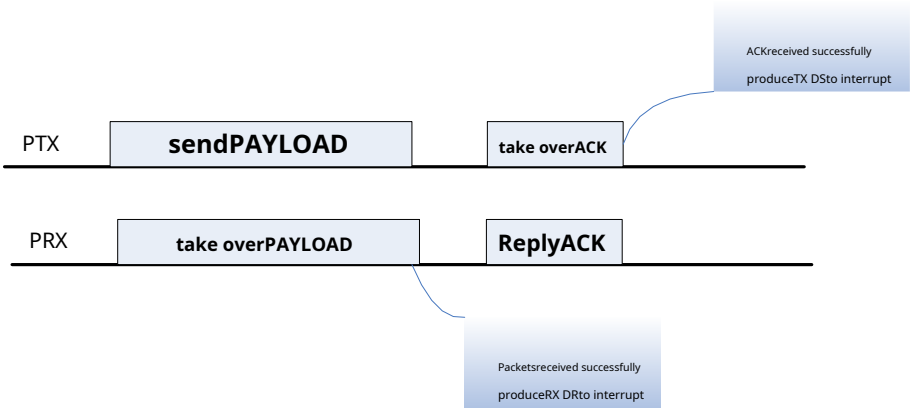
4.2.1 ACKmodel

when usedW_TX_PAYLOADcommand to senderTX FIFOWhen writing data, after packing the data, the packet control field in the data packetNO_ACKThe flag bit is reset. After the receiver receives a frame of valid data, it generatesRX_DRAfter an interrupt, a frame is automatically sentACKsignal, the sender receivesACKsignal, it is automatically clearedTX FIFOdata and generateTX_DSThe transmission was interrupted, indicating that the communication was successful.

The receiver is sendingACKWhen signaling, take the receiving pipe address as the target address to sendACKsignal, so the sender needs to set up the receive pipeline0The address is the same as its own sending address for receivingACKSignal.

If the sender is inARDnot received in timeACKsignal, resend the previous frame of data. When the number of retransmissions reaches the maximum and no acknowledgment signal is received, the sender generatesMAX_RTinterruption.MAX_RTThe next step of data transmission cannot be performed before the interrupt is cleared. All interrupts are cleared by writing to the status register.PLOS_CNT register generates aMAX_RTadd after interruption1, used to record the number of lost data packets in the current frequency band. ARC_CNTThe register records the number of retransmissions of the current data, and resets it when a packet of new data is sent. The maximum number of retries andARDtime passesSETUP_RETRregisters for configuration. Automatically reply on the receiving endACK signal byEN_AAregister to control.

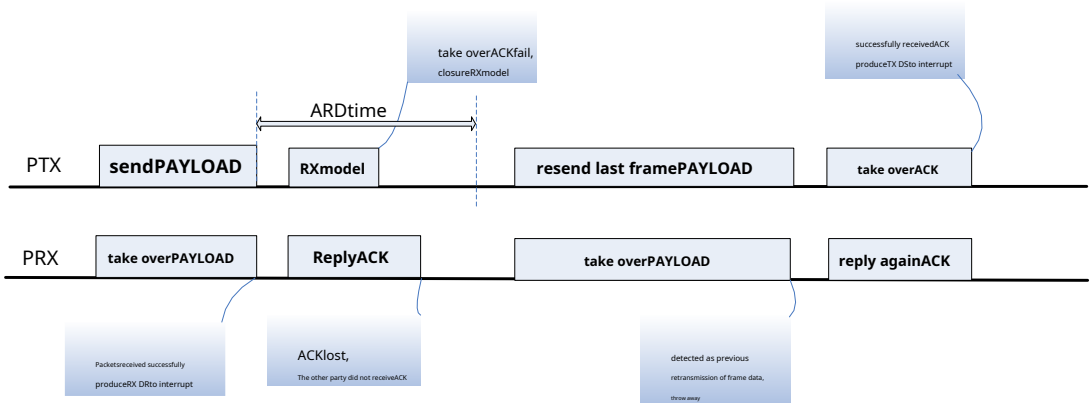
picture4-3shown asACKA communication in the mode is completed.



picture4-3 ACKcommunication mode

Whenever the sender transmits a new data packet, the correspondingPIDsAutomatically add1, so in the two adjacent data packets sent,PIDsshould be different from each other. If several consecutive frames of data in the link are lost, the number of consecutive two frames of data received by the receiving end PIDsProbably the same.

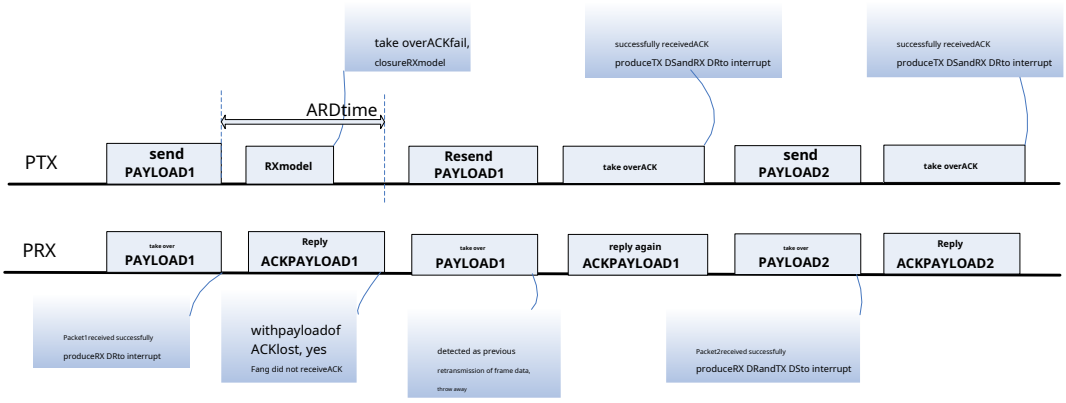
If the receiving end finds that the received data is the same as the previous frame dataPIDssame, then compareCRC,ifCRCAlso the same, it is judged as the retransmission of the previous frame data, discard the data, and reply againACKSignal. picture4-4The sender did not receive the first data transmissionACKsignal, after retransmission, is receivedACKsignal, data communication completed successfully.



picture4-4noneACK PAYLOADcommunication mode

The receiver is replyingACKsignal, it is possible to simultaneously send aACKSignal(ACKPAYLOAD). Enabling this feature requires configurationFETUREin the registerEN_ACK_PAYbit, and both parties must enable dynamic payload length.

receiver firstW_ACK_PAYLOADrightTX FIFOWrite to the corresponding receiving data pipeline ACKPAYLOAD, when this pipeline receives a new frame of valid data, it generatesRX_DRInterrupt, and auto-replyACK, and automatically ACKPAYLOADIt is packaged and sent to the sender; the sender receives the payload dataACKAfter the signal is generated simultaneouslyTX_DSandRX_DRinterruption. When the receiving end receives a packet of valid data sent by the sending end again, it means that the sending end has receivedACKPAYLOAD, clearTX FIFOin the data, while generatingRX_DRand TX_DSinterruption. If the received data is a retransmission of the previous packet of data, retransmit this ACKPAYLOAD packaged asACKThe signal is sent out. picture4-5The sender did not receive the message withACKPAYLODofACKsignal, retransmit, and the receiving end sends thisACKPAYLOADPacking, after the receiving end receives it, send the next frame of data.



picture4-5bringACK PAYLOADcommunication mode

4.2.2 NO ACKmodel

useW_TX_PAYLOAD_NOACKcommand write to the senderTX PAYLOAD, in the packet NO_ACKThe flag bit is set to1, after the sending end sends a packet of data, it will generate immediatelyTX_DSInterrupt, and start preparing to send the next packet of data. The receiving end judges after receiving the dataNO_ACKflag is set and the data is valid, aRX_DRInterrupt, at this time a frame of data communication is completed, no replyACKSignal. W_TX_PAYLOAD_NOACKorder passedFETUREin the registerEN_DYN_ACKto enable.

4.2.3dynamicPAYLOADlength and staticPAYLOADlength

The sender configuresFEATUREin the registerEN_DPLBit andDYNPDin the registerDPL_P0 bit, enter the dynamic payload length mode, the packet control field in the sent data packet6The bit is the length of the data to be sent

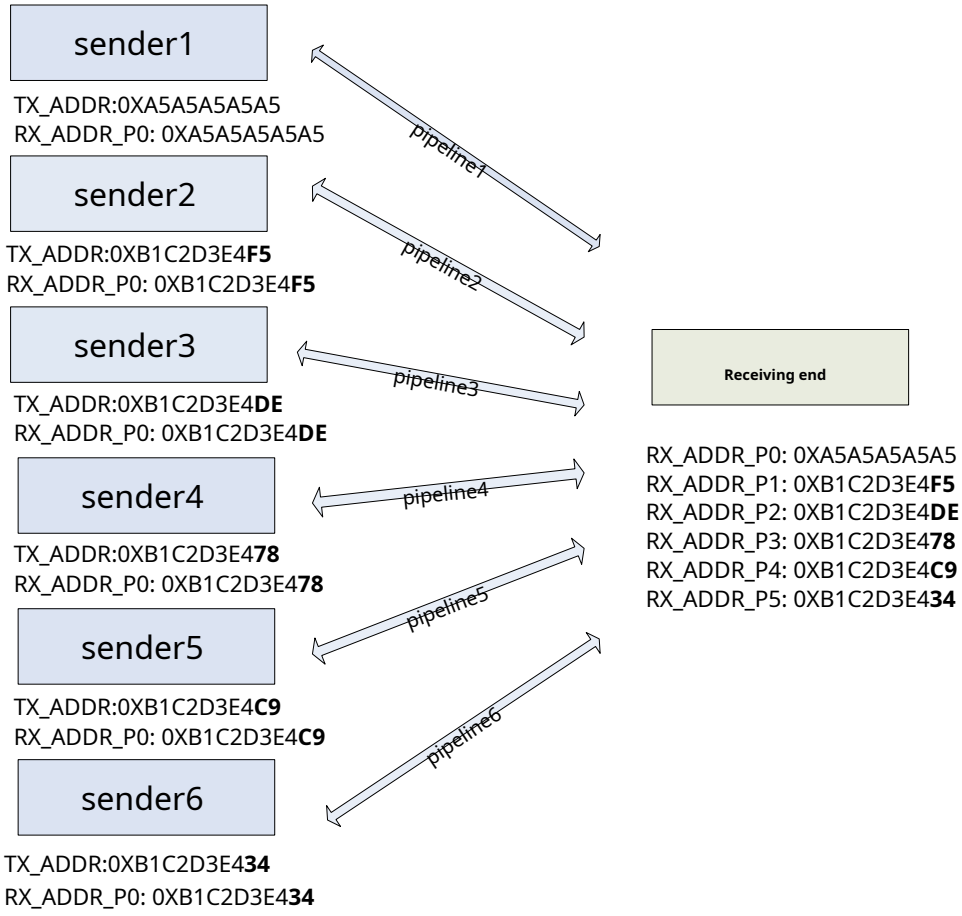
receiver configurationFEATUREin the registerEN_DPLbit, and turn onDYNPDAfter the dynamic enable of the corresponding pipeline in the register, the data is automatically received with the data length in the packet control word in the data packet. Therefore, the length of the payload data received each time can be different, and can be passedR_RX_PL_WIDcommand to read the length of the payload data. If the default is the static payload length, the payload length of each transmission at the sender must be the same, and must be the same as that configured by the receiver in advance.RX_PW_PxThe register values are the same.

4.2.4multi-channel communication

Transceivers can be simultaneously6sender,1Two-way or one-way communication between two receivers. At this point, the receiver must EN_RXADDREnable each pipeline in the register, and set the address of each receiving pipeline to be the same as the sending address of the corresponding sending end. which receives the pipeline0have separate5byte address, pipe1-5shared high4byte effective address.

If the transmitter needs to receiveACKsignal, you also need to set up its receiving pipeline0The address is the same as the sending address of itself.

In the multi-channel communication mode, the address setting reference diagram of the sender and receiver4-6.



picture4-6multi-channel communication pattern

Up to1:6star network.

5 SPIData and Control Interface

The chip uses a standard four-wireSPIInterface, the measured maximum reading and writing speed is greater than10Mb/S. An external microcontroller can beSPIThe interface configures the chip, including reading and writing function registers, reading and writingFIFO, read chip status, clear interrupts, etc.

5.1 SPIOrder

SPIcommand see table5-1.CSNtoggle from high to low,SPIThe interface starts working. every timeSPI operate,MISOThe first byte of the output is the value of the status register, and then the command is used to determine whether to output the value (no output is a high-impedance state). In the command format, the command word is pressed fromMSBitarriveLS BitEnter in the order of the data format according to from LSByte arriveMSBytein order, per byte in order fromMSBitarriveLS Bitinput in sequence. For details, please refer toSPI Timing, Diagram5-1and diagram5-2.

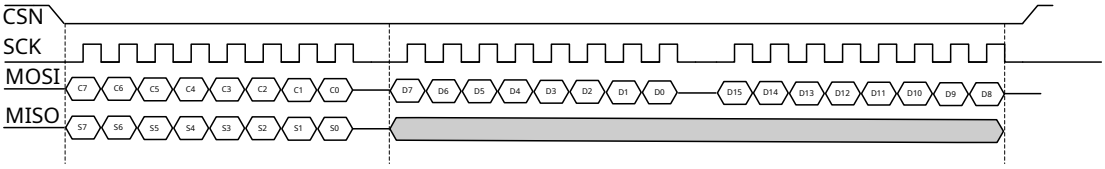
surface5-1

Command name	Command word (binary)	# Data bytes	operate
R_REGISTER	000A AAAA	1 to 5 LSByte first	read register command,AAAAAIndicates the register address (refer to register table).
W_REGISTER	001A AAAA	1 to 5 LSByte first	write register command,AAAAAIndicates the register address (refer to Register Table), only allowShutdown, Standby,Idle-TXmode to operate.
R_RX_PAYLOAD	0110 0001	1 to 32 LSByte first	FromFIFORead the received data in,1-32bytes, after readingFIFOData is deleted. Applies to receive mode.
W_TX_PAYLOAD	1010 0000	1 to 32 LSByte first	Write launch payload data, size is1-32bytes, applicable in transmit mode.
FLUSH_TX	1110 0001	0	emptyTX FIFO, for launch mode.
FLUSH_RX	1110 0010	0	emptyRX FIFO, for receive mode. back if necessaryACK, you cannot returnACKClear before operation completesFIFO, otherwise it is considered a communication failure.
REUSE_TX_PL	1110 0011	0	Apply to sender, clearTX FIFOor rightFIFOThis command cannot be used after writing new data.
R_RX_PL_WID	0110 0000	1	Read the number of data bytes received.
W_ACK_PAYLOAD	1010 1PPP	1 to 32 LSByte first	Applied to the recipient, viaPIPE PPPPass the data through ACKsent out in the form of up to three frames of data storage AtFIFOmiddle.
W_TX_PAYLOAD_NO ACK	1011 0000	1 to 32 LSByte first	Applicable to launch mode, using this command also requires WillAUTOACKLocation1.
NOP	1111 1111	0	No action. available for returnSTATUSvalue.

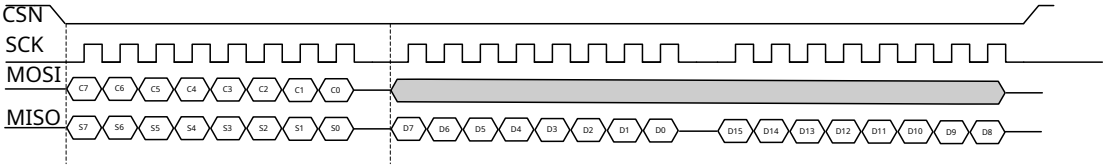
5.2 SPItiming

SPIOperations include basic read and write operations and other command operations, as shown in the timing diagram5-1and diagram5-2.

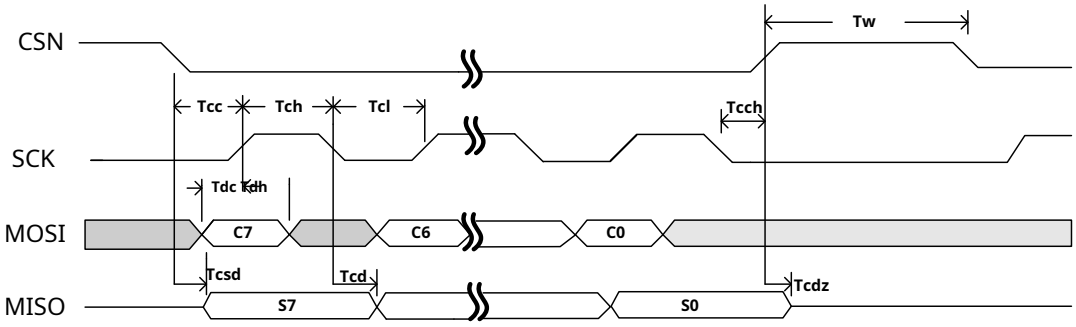
Note: only inShutdown,StandbyandIdle-TXOnly in this mode can the registers be configured.



picture5-1 SPIwrite operation



picture5-2 SPIread operation



picture5-3 SPIstypical timing

surface5-1forSPITypical timing parameters.

surface5-1 SPItiming parameters

Symbol	Parameters	Min	Max	Units
Tdc	Data to SCK Setup	2		ns
Td	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		42	ns
Tcd	SCK to Data Valid		58	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	10	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tw	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		42	ns

6Register Mapping Table

address (Hex)	Mnemonic	bit	Reset Value	type	Description
00	CONFIG				configuration register
	Reserved	7	0	R/W	reserve,0
	MASK_RX_DR	6	0	R/W	Receive interrupt mask control 0: Receive interrupt enable,RX_DRinterrupt flag at IRQAn interrupt signal is generated on the pin, active low 1: receive interrupt off,RX_DRInterrupt flags do not affectIRQpin out
	MASK_TX_DS	5	0	R/W	Transmit Interrupt Mask Control 0: transmit interrupt enable,TX_DSinterrupt flag at IRQAn interrupt signal is generated on the pin, active low 1: transmit interrupt off,TX_DSInterrupt flags do not affectIRQpin out
	MASK_MAX_RT	4	0	R/W	Maximum retransmission count interrupt mask control 0: Maximum retransmission count interrupt enable,MAX_RT interrupt flag atIRQAn interrupt signal is generated on the pin, active low 1: maximum retransmission count interrupt off,MAX_RT Interrupt flags do not affectIRQpin out
	EN_CRC	3	1	R/W	EnableCRC. ifEN_AAnot all zeros, EN_CRCmust be1. 0:closureCRC 1: openCRC
	CRCO	2	0	R/W	CRClength configuration, 0:1byte 1:2 bytes
	PWR_UP	1	0	R/W	Power-off/power-on mode configuration 0: shutdown mode 1: boot mode
	PRIM_RX	0	0	R/W	transmit/receive configuration, only in theShutdownand Standbychange under 0: launch mode 1: Receive mode
01	EN_AA				Enable auto-acknowledgement
	Reserved	7:6	00	R/W	reserve,00
	ENAA_P5	5	1	R/W	Enable data pipeline5auto confirm

	ENAA_P4	4	1	R/W	Enable data pipeline4auto confirm
	ENAA_P3	3	1	R/W	Enable data pipeline3auto confirm
	ENAA_P2	2	1	R/W	Enable data pipeline2auto confirm
	ENAA_P1	1	1	R/W	Enable data pipeline1auto confirm
	ENAA_P0	0	1	R/W	Enable data pipeline0auto confirm
02	EN_RXADDR				Enable receive data pipe address
	Reserved	7:6	00	R/W	reserve,00
	ERX_P5	5	0	R/W	Enable data pipeline5
	ERX_P4	4	0	R/W	Enable data pipeline4
	ERX_P3	3	0	R/W	Enable data pipeline3
	ERX_P2	2	0	R/W	Enable data pipeline2
	ERX_P1	1	1	R/W	Enable data pipeline1
	ERX_P0	0	1	R/W	Enable data pipeline0
03	SETUP_AW				Address Width Configuration
	Reserved	7:2	000000	R/W	reserve,000000
	AW	1:0	11	R/W	Transmitter/Receiver Address Width 00: error value 01:3bytes 10:4bytes 11:5bytes
04	SETUP_RETR				Auto-Resend Configuration
	ARD	7:4	0000	R/W	Automatic retransmission delay configuration 0000:250uS 0001:500uS 0010:750uS … 1111:4000uS
	ARC	3:0	0011	R/W	Maximum number of automatic retransmissions 0000: Disable auto-resend 0001:1Second-rate 0010:2Second-rate … 1111:15Second-rate
05	RF_CH				RF channel
	Reserved	7	0	R/W	reserve,0
	RF_CH	6:0	0000010	R/W	Set the channel when the chip is working, corresponding to the first 0~125channels; the channel interval is1MHz,The default is02which is2402MHz

06	RF_SETUP				RF configuration
	CONT_WAVE	7	0	R/W	for'1'When the constant carrier transmission mode is enabled, it is used to Test transmit power
	Reserved	6	0	R/W	reserve,0
	RF_DR_LOW	5	0	R/W	Set the RF data rate to250kbps,1Mbpsor 2Mbps,andRF_DR_HIGHjoint control
	PLL_LOCK	4	0	R/W	Reserved words, must be0
	RF_DR_HIGH	3	1	R/W	Set RF data rate [RF_DR_LOW, RF_DR_HIGH]: 00:1Mbps 01:2Mbps 10:250kbps 11:reserve
	RF_PWR	2:0	110	R/W	set upTXtransmit power 111: 7dBm 110: 4dBm 101: 3dBm 100: 1dBm 011: 0dBm 010: -4dBm 001: -6dBm 000:-12dBm
07	STATUS				status register (SPIThe first byte of the operation, status state register value through theMISOserial output).
	Reserved	7	0	R/W	reserve,0
	RX_DR	6	0	R/W	RX FIFOValue flag, write'1'clear.
	TX_DS	5	0	R/W	Transmitter transmit complete interrupt bit, if it isACK mode, you receiveACKAfter confirming the signal TX_DS Location'1',Write'1'clear.
	MAX_RT	4	0	R/W	Reach the maximum number of retransmission interrupt bit, write'1'clear.
	RX_P_NO	3:1	111	R	Receive pipeline for receiving dataPPPnumber, you can pass SPIread out. 000-101: data pipeline0-5 110:unavailable 111:RX FIFOIs empty
	TX_FULL	0	0	R	TX FIFOfull flag.
08	OBSERVE_TX				launch result statistics
	PLOS_CNT	7:4	0	R	Packet count. The maximum count is15,ChangeRF_CH rear PLOS_CNTFrom0Start counting.
	ARC_CNT	3:0	0	R	Retransmission count. When emitting a new package,ARC_CNTFrom0Start counting.

09	RSSI				Received signal strength detection
	Reserved	7:1	000000	R	
	RSSI	0	0	R	Received signal strength:0: The received signal is less than <-60dBm
0A	RX_ADDR_P0	39:0	0xE7E7E7E7E7	R/W	data pipeline0Receive address for , with a maximum width of 5bytes (LSBytefirst written, via SETUP_AWconfigure address width).
0B	RX_ADDR_P1	39:0	0xC2C2C2C2C2	R/W	data pipeline1Receive address for , with a maximum width of 5bytes (LSBytefirst written, via SETUP_AWconfigure address width).
0C	RX_ADDR_P2	7:0	0xC3	R/W	data pipeline2The lowest byte of the receive address, followed by Receive address high byte andRX_ADDR_P1[39:8] same.
0D	RX_ADDR_P3	7:0	0xC4	R/W	data pipeline3The lowest byte of the receive address, followed by Receive address high byte andRX_ADDR_P1[39:8] same.
0E	RX_ADDR_P4	7:0	0xC5	R/W	data pipeline4The lowest byte of the receive address, followed by Receive address high byte andRX_ADDR_P1[39:8] same.
0F	RX_ADDR_P5	7:0	0xC6	R/W	data pipeline5The lowest byte of the receive address, followed by Receive address high byte andRX_ADDR_P1[39:8] same.
10	TX_ADDR	39:0	0xE7E7E 7E7E7	R/W	The launch address of the sender (LSBytefirst written) , If the launch needs to receiveACKconfirmation signal, then Need to configureRX_ADDR_P0The value is equal to TX_ADDR, and enableARQ.
11	RX_PW_P0				
	Reserved	7:6	00	R/W	reserve
	RX_PW_P0	5:0	0	R/W	receive data pipeline0data bytes (1—32Bytes). 1:1byte … 32:32bytes

12	RX_PW_P1				
	Reserved	7:6	00	R/W	reserve
	RX_PW_P1	5:0	0	R/W	receive data pipeline1data bytes (1—32Bytes). 1:1byte … 32:32bytes
13	RX_PW_P2				
	Reserved	7:6	00	R/W	reserve
	RX_PW_P2	5:0	0	R/W	receive data pipeline2data bytes (1—32Bytes). 1:1byte … 32:32bytes
14	RX_PW_P3				
	Reserved	7:6	00	R/W	reserve
	RX_PW_P3	5:0	0	R/W	receive data pipeline3data bytes (1—32Bytes). 1:1byte … 32:32bytes
15	RX_PW_P4				
	Reserved	7:6	00	R/W	reserve
	RX_PW_P4	5:0	0	R/W	receive data pipeline4data bytes (1—32Bytes). 1:1byte … 32:32bytes
16	RX_PW_P5				
	Reserved	7:6	00	R/W	reserve
	RX_PW_P5	5:0	0	R/W	receive data pipeline5data bytes (1—32Bytes). 1:1byte … 32:32bytes
17	FIFO_STATUS				FIFOstate
	Reserved	7	0	R/W	reserve,0

	TX_REUSE	6	0	R	Only for the transmitter,FIFOdata reuse when usedREUSE_TX_PLAfter the command, transmit the data that has been successfully transmitted last time, by W_TX_PAYLOADorFLUSH TXcommand to disable the function
	TX_FULL	5	0	R	TX FIFOfull sign 1:TX FIFOFull 0:TX FIFOwritable
	TX_EMPTY	4	1	R	TX FIFOempty sign 1:TX FIFOIs empty 0:TX FIFOhave data
	Reserved	3:2	00	R/W	reserve,00
	RX_FULL	1	0	R	RX FIFOfull sign 1:RX FIFOFull 0:RX FIFOwritable
	RX_EMPTY	0	1	R	RX FIFOempty sign 1:RX FIFOIs empty 0:RX FIFOhave data
1C	DYNPD				Enable dynamic payload length
	Reserved	7:6	0	R/W	reserve,00
	DPL_P5	5	0	R/W	Enable receive pipeline5Dynamic load length (need EN_DPLandENAA_P5).
	DPL_P4	4	0	R/W	Enable receive pipeline4Dynamic load length (need EN_DPLandENAA_P4).
	DPL_P3	3	0	R/W	Enable receive pipeline3Dynamic load length (need EN_DPLandENAA_P3).
	DPL_P2	2	0	R/W	Enable receive pipeline2Dynamic load length (need EN_DPLandENAA_P2).
	DPL_P1	1	0	R/W	Enable receive pipeline1Dynamic load length (need EN_DPLandENAA_P1).
	DPL_P0	0	0	R/W	Enable receive pipeline0Dynamic load length (need EN_DPLandENAA_P0).
1D	FEATURE			R/W	feature register
	Reserved	7:3	0	R/W	reserve,00000
	EN_DPL	2	0	R/W	Enable dynamic payload length
	EN_ACK_PAY	1	0	R/W	EnableACKpayload (with payload dataACKBag)
	EN_DYN_ACK	0	0	R/W	enable commandW_TX_PAYLOAD_NOACK

7Main parameter index

7.1Limit parameter

working conditions	minimum value	maximum value	unit
voltage			
VDD	- 0.3	3.6	V
VSS		0	V
Input voltage			
VI	- 0.3	5.25	V
The output voltage			
VO	VSS to VDD	VSS to VDD	V
total power consumption			
		100	mW
temperature			
range of working temperature	- 40	+85	℃
storage temperature	- 40	+ 125	℃
ESDperformance	HBM (Human Body Model): Class 1C		

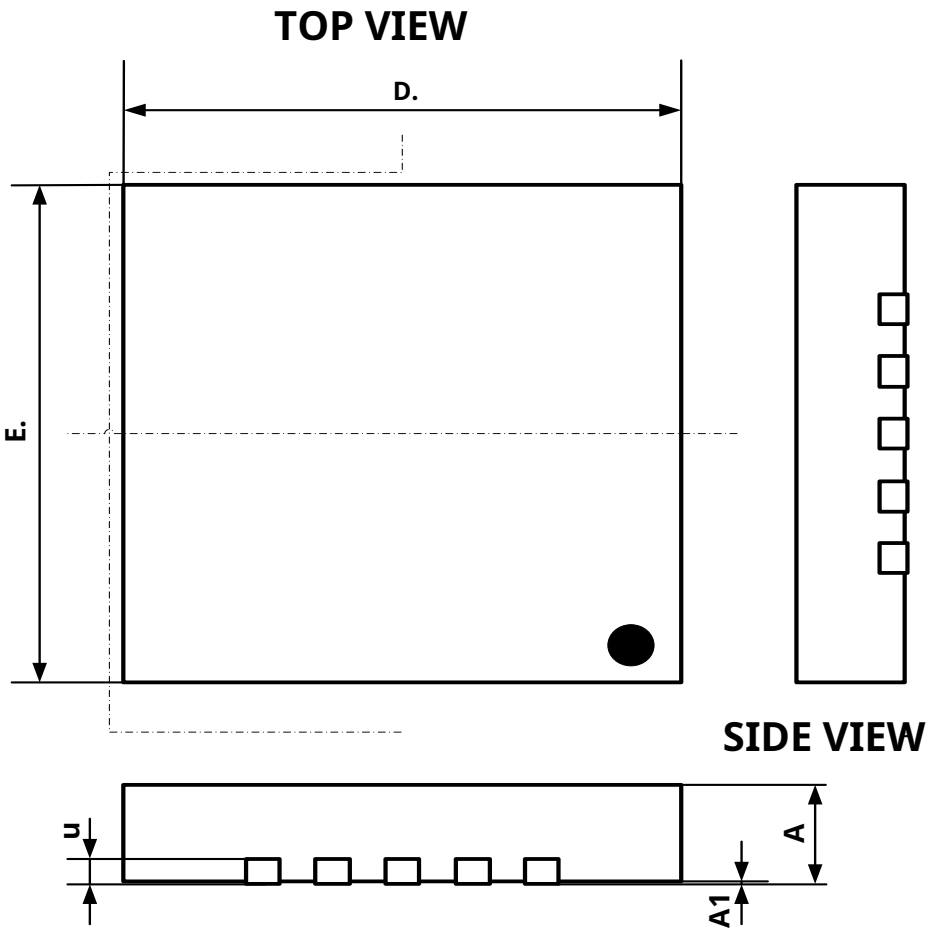
7.2Electrical indicators

condition:VDD=3V, VSS=0V TA=27℃,crystal oscillatorCL=12pF

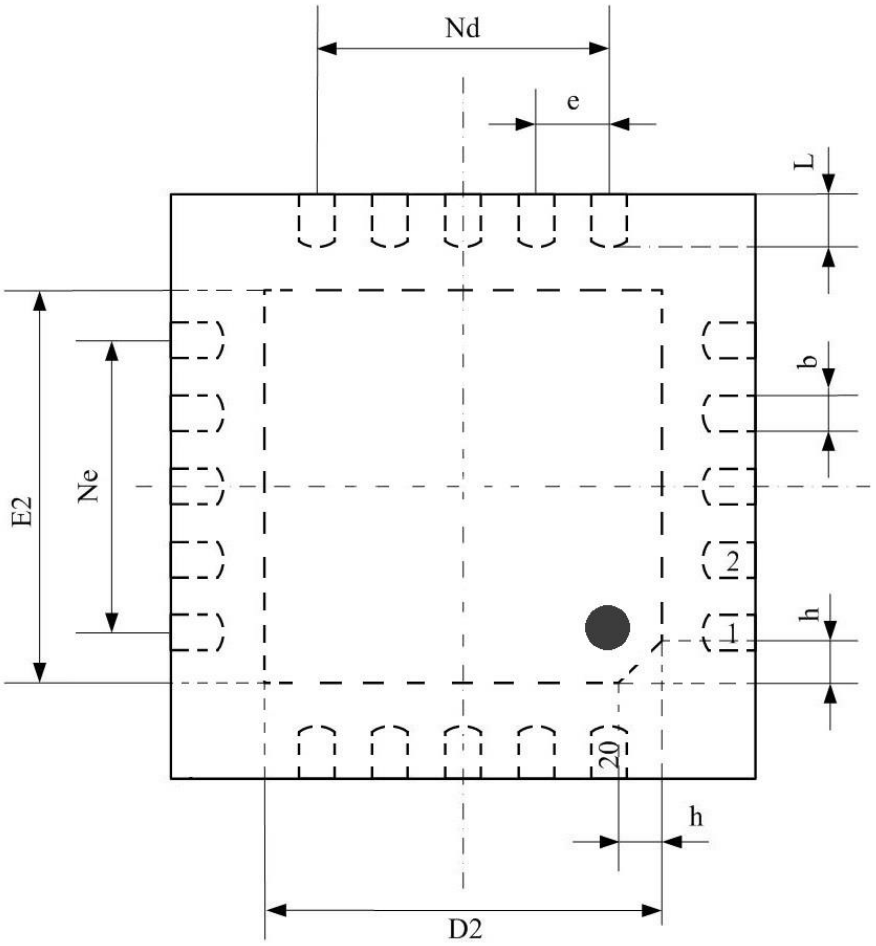
symbol	parameter	minimum value	typical value	maximum value	unit	Remark
OPparameter						
VDD	Power supply voltage range	1.9		3.6	V	
I_{SHD}	ShutdownMode current		1		μA	
I_{STB}	StandbyMode current		15		μA	
I_{IDLE}	Idle-TXMode current		380		μA	
I_{RX}@2MHZ	RXMode current @2Mbps		15		mA	
I_{RX}@1MHZ	RXMode current @1Mbps		14.5		mA	
I_{RX}@250kbps	RXMode current @250kbps		14		mA	
I_{TX}@7dBm	TXMode current @7dBm		25		mA	
I_{TX}@4dBm	TXMode current @4dBm		16		mA	
I_{TX}@0dBm	TXMode current @0dBm		12		mA	

I_{TX}@-6dBm	TXMode current @-6dBm		9.5		mA	
I_{TX}@-12dBm	TXMode current @-12dBm		8.5		mA	
RFparameter						
f_{OP}	RFFrequency Range	2400		2525	MHz	
f_{CH}	RFchannel spacing	1			MHz	2Mpbstime to less for2MHz
ΔF_{MOD}(2Mbps)	Modulation Frequency Offset		±330		KHz	
ΔF_{MOD}(1M/250Kbps)	Modulation Frequency Offset		±175		KHz	
R_{GFSK}	data rate	250		2000	Kbps	
RXparameter						
RX_{SENS}@2Mbps	Sensitivity@2Mbps		- 83		dBm	BER=0.1%
RX_{SENS}@1Mbps	Sensitivity@1Mbps		- 87		dBm	BER=0.1%
RX_{SENS}@250Kbps	Sensitivity@250kbps		-96		dBm	BER=0.1%
C/I_{CO}@2Mbps	co-channel selectivity		6		dB	
C/I_{1st}@2Mbps	1st adjacent channel selectivity 2MHz		0		dB	
C/I_{2ND}@2Mbps	2nd adjacent channel selectivity 4MHz		- 20		dB	
C/I_{3rd}@2Mbps	3rd adjacent channel selectivity 6MHz		- 26		dB	
C/I_{CO}@1Mbps	co-channel selectivity		7		dB	
C/I_{1st}@1Mbps	1st adjacent channel selectivity 2MHz		6		dB	
C/I_{2ND}@1Mbps	2nd adjacent channel selectivity 4MHz		- twenty one		dB	
C/I_{3rd}@1Mbps	3rd adjacent channel selectivity 6MHz		- 30		dB	
TXparameter						
P_{RF}	RFOutput Power	- 30		7	dBm	
P_{BW}@2Mbps	modulation bandwidth		2.1		MHz	
P_{BW}@1Mbps	modulation bandwidth		1.1		MHz	
P_{BW}@250Kbps	modulation bandwidth		0.9		MHz	
P_{RF1}	1stadjacent channel power2MHz			- 20	dBm	
P_{RF2}	2ndadjacent channel power4MHz			- 46	dBm	
Crystal parameters						
f_{XO}	Crystal frequency		16		MHz	
ΔF	frequency deviation		±60		ppm	
ESR	Equivalent loss resistance		100		Ω	

8encapsulation



picture8-1top level map

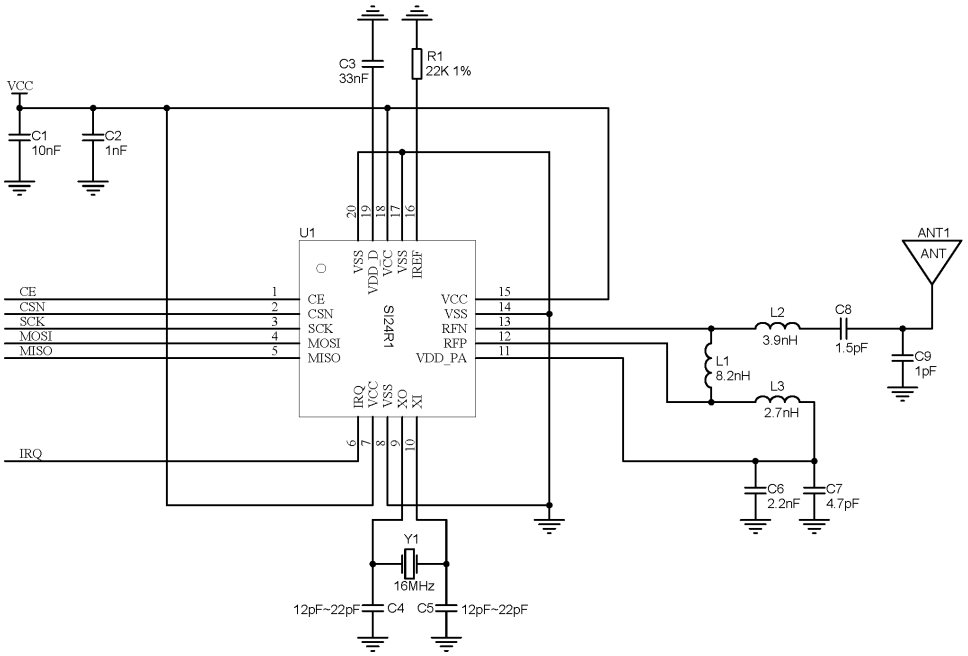


picture8-2Package Dimensions (Top View-top view)

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
D.	3.90	4.00	4.10
D2	2.55	2.65	2.75
e	0.50BSC		
E2	2.55	2.65	2.75
E.	3.90	4.00	4.10
Ne	2.00BSC		
Nd	2.00BSC		
L	0.35	0.40	0.45
h	0.30	0.35	0.40
u	0.20 REF.		
L/FCarrier size (mil)	114×114		

9Typical Application Schematic

9.1Typical Application Schematic



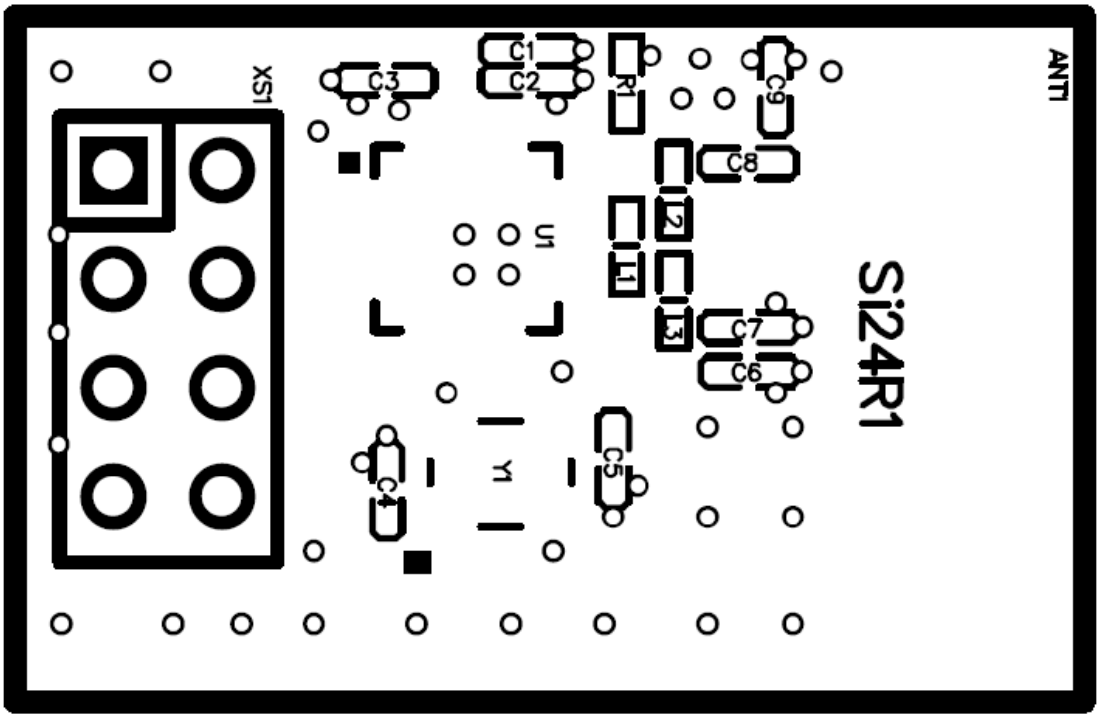
picture9-1Typical Application Schematic

surface9-1componentsBOMsurface

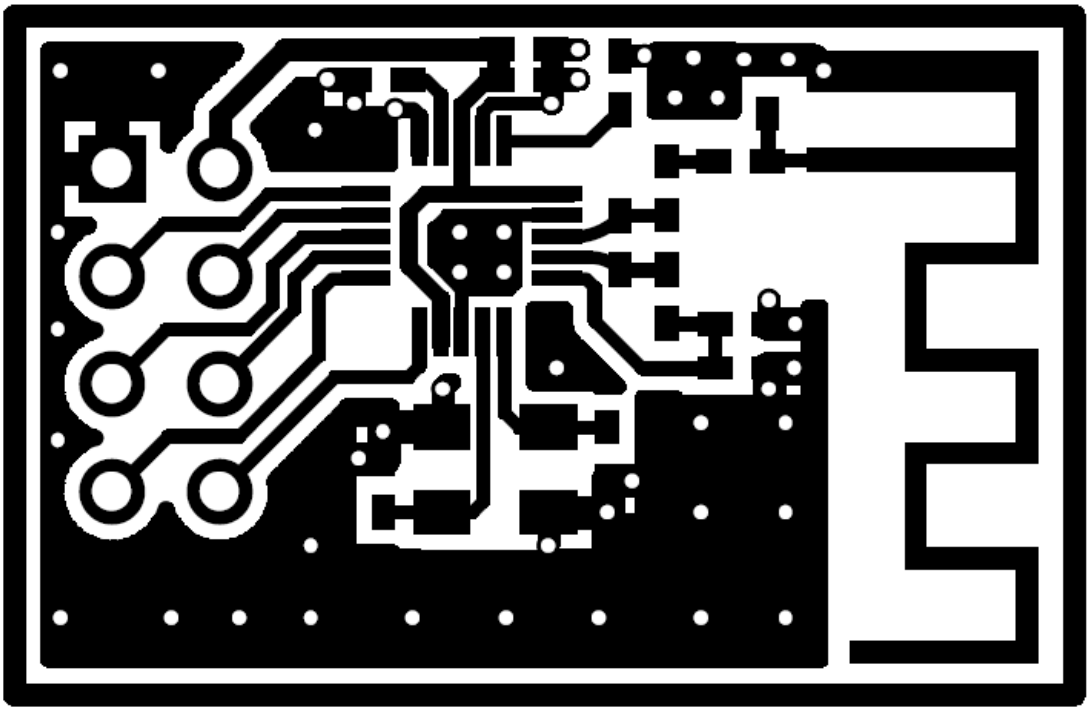
Device name	value	form	describe
C1	10nF	0402	X7R, +/- 10%
C2	1nF	0402	X7R, +/- 10%
C3	33nF	0402	X7R, +/- 10%
C4	12~22pF	0402	NPOs, +/- 2%
C5	12~22pF	0402	NPOs, +/- 2%
C6	2.2nF	0402	X7R, +/- 10%
C7	4.7pF	0402	NPO, +/- 0.25pF
C8	1.5pF	0402	NPO, +/- 0.1pF
C9	1.0pF	0402	NPO, +/- 0.1pF
L1	8.2nH	0402	chip inductor, +/- 5%
L2	3.9nH	0402	chip inductor, +/- 5%
L3	2.7nH	0402	chip inductor, +/- 5%
R1	22KΩ	0402	+/- 1%
R2	Not mounted	0402	
Y1	16MHz		+ /-60ppm, CL=12pF
U1		QFN20 04×04	

9.2 PCBwiring

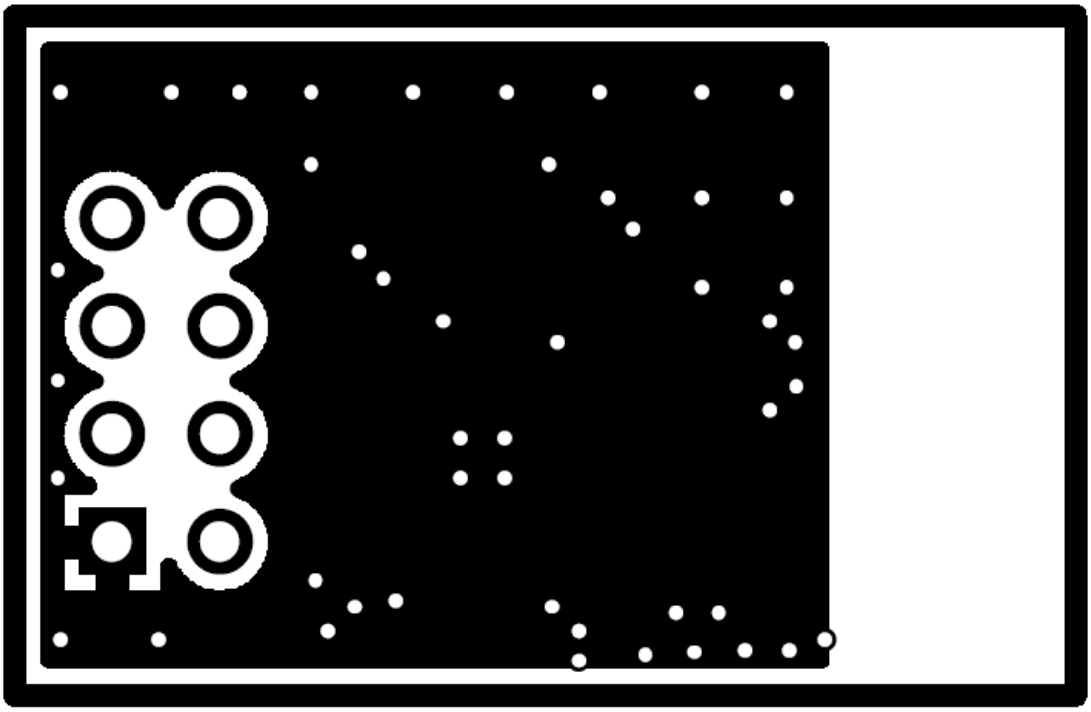
As shown in the figure belowPCBThe wiring is typical of the schematic diagram above for the circuitPCBWiring example, here'sPCBBoards are FR-4Double-sided board, there is a copper clad surface on the top layer and the bottom layer respectively, the copper clad surface of the top layer and the bottom layer are connected by a large number of via holes, and there is no copper clad surface under the antenna. The bottom of the chip is ground, in order to ensure betterRFperformance, recommended chip bottom Die ExposedandPCBConnected on a large scale.



picture9-2On-chip antenna top layer silkscreen (0402element)



picture9-3On-Chip Antenna Top Layer Layout Diagram (0402element)



picture9-4On-chip antenna bottom layer wiring diagram

10Version Information

Version	modified date	Modify content
V1.0	2021/12/02	Modify contact information

11order information

Package mark

Si24R1
ABBCDEE

Si24R1+:chip code

A:encapsulation date year code,5represent2020year

BB:Processing and issuing weekly records, for example42representative isAof the year42Weekly processing

C:package factory code, forA,HT,NJorWA, also abbreviated asA,h,NorWD:test factory code, forA,Z,orHEE:production batch code

surface11-1Order Information Form

order code	encapsulation	Package	smallest unit
Si24R1-Sample	4×4mm 20-pin QFN	Box/Tube	5
Si24R1-P	4×4mm 20-pin QFN	Tray	1K
Si24R1-P	4×4mm 20-pin QFN	Tape and reel	4K

12Technical support and contact information

Nanjing Zhongke Microelectronics Co., Ltd. Technical Support Center

Telephone:025-68517780

address:R&D Zone 3, Xuzhuang Software Park, Xuanwu District, NanjingBBuilding201

Sale

cell phone:18961759481

Mail:sales@csmic.ac.cn

Technical Support

cell phone:13645157034

Mail:supports@csmic.ac.cn

URL:http://www.csm-ic.com

Attachment: Typical Configuration Scheme

Mode one:ACKcommunication

Transmitter configuration:

```
spi_rw_reg(SETUP_AW, 0x03); spi_write_buf(TX_ADDR, //Set the address width to5bytes
TX_ADDRESS, 5); spi_write_buf(RX_ADDR_P0, TX_ADDRESS, //Write the sending address,5byte
5); spi_write_buf(W_TX_PAYLOAD, buf, TX_PLOAD_WIDTH); //receiving channel0The address is the same as the transmit address
                                                      //WriteTX FIFO
                                                      //Enable dynamic payload length
spi_rw_reg(DYNPD, 0x01);          //turn onDPL_P0
spi_rw_reg(SETUP_RETR, 0x15);     //Automatic retransmission delay waiting500us,automatic resend5
spi_rw_reg(RF_CH, 0x40);          Second-rate //Select RF channel
spi_rw_reg(RF_SETUP, 0x0e);       //data transfer rate2Mbpsand power
spi_rw_reg(CONFIG, 0x0e); CE =    //configured in transmit mode,CRC, maskable interrupt
1;
```

Receiver configuration:

```
spi_write_buf(RX_ADDR_P0, TX_ADDRESS, 5);   //receiving channel0The address is the same as the transmit address
spi_rw_reg(EN_RXADDR, 0x01);      //Enable receive channel0
spi_rw_reg(RF_CH, 0x40);          //Select RF channel
spi_rw_reg(SETUP_AW, 0x03);       //Set the address width to5bytes
spi_rw_reg( FEATURE, 0x04);       //Enable dynamic load
spi_rw_reg(DYNPD, 0x01);          //turn onDPL_P0
spi_rw_reg(RF_SETUP, 0x0e);       //data transfer rate2Mbpsand power
                                  //configured in receive mode,CRC, maskable interrupt
```

Mode two:NOACKcommunication

Transmitter configuration:

```
spi_write_buf( TX_ADDR, TX_ADDRESS, 5);          //Write sending address
spi_rw_reg( FEATURE, 0x01); //EnableW_TX_PAYLOAD_NOACKOrder
spi_write_buf(W_TX_PAYLOAD_NOACK, buf, TX_PLOAD_WIDTH);          //WriteFIFO
spi_rw_reg(SETUP_AW, 0x03);       // 5 byte Address
spi_rw_reg( RF_CH, 0x40);         width //Select RF channel0x40
spi_rw_reg(RF_SETUP, 0x08);       //data transfer rate2Mbps
spi_rw_reg( CONFIG, 0x0e); CE     //configured in transmit mode,CRCfor2Bytes
= 1;
```

Receiver configuration:

```
spi_write_buf( RX_ADDR_P0, TX_ADDRESS, 5);      //receiving address
spi_rw_reg( EN_RXADDR, 0x01);       //Enable receive channel0
spi_rw_reg( RF_CH, 0x40);                 //Select RF channel
spi_rw_reg( RX_PW_P0, TX_PLOAD_WIDTH);          //set receive channel0Payload Data
spi_rw_reg( RF_SETUP, 0x08);                Width //data transfer rate2Mbps,-18dbm TX power
spi_rw_reg( CONFIG, 0x0f);        //configured as receiver,CRCfor2Bytes
CE = 1;
```

Mode 3: The receiver opens multiple channels

Dynamic load:

```
spi_rw_reg(FEATURE, 0x04);
spi_rw_reg(DYNPD, 0x3F) ;      //Enable dynamic payload length for all channels
spi_rw_reg(EN_RXADDR, 0x3F);          //open all channels
spi_rw_reg(RF_CH, 0x40);         //Select RF channel0x40
spi_rw_reg(SETUP_AW, 0x03);      // 5 byte Address width //
spi_rw_reg(CONFIG, 0x0B); CE    configured as receiver
= 1;
```

static load:

```
spi_rw_reg(RX_PW_P0, 0x20);      //set channel0Receive data width
spi_rw_reg(RX_PW_P1, 0x20);
spi_rw_reg(RX_PW_P2, 0x20);
spi_rw_reg(RX_PW_P3, 0x20);
spi_rw_reg(RX_PW_P4, 0x20);
spi_rw_reg(RX_PW_P5, 0x20);

spi_rw_reg(EN_RXADDR, 0x3F);        //open all channels
spi_rw_reg(RF_CH, 0x40);          //Select RF channel0x40
spi_rw_reg(SETUP_AW, 0x03);      //set address width
spi_rw_reg(CONFIG, 0x0F); CE    //configured as receiver
= 1;
```